Gate Dielectric Integrity

MATERIAL, PROCESS, AND TOOL QUALIFICATION

Dinesh C. Gupta and
George A. Brown, editors

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Peer Review Policy

Each paper published in this volume was evaluated by two peer reviewers and the editor. The authors addressed all of the reviewers' comments to the satisfaction of both the technical editor(s) and the ASTM Committee on Publications.

The quality of the papers in this publication reflects not only the obvious efforts of the authors and the technical editor(s), but also the work of the peer reviewers. In keeping with long standing publication practices, ASTM maintains the anomymity of the peer reviewers. The ASTM Committee on Publications acknowledges with appreciation their dedication and contribution of time and effort on behalf of ASTM.

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Foreword

The Conference on Gate Dielectric Integrity was held on January 25, 1999 in San Jose, California. ASTM Committee F-1 on Electronics sponsored the conference. The conference co-chairmen were Dinesh Gupta, of Mitsubishi Silicon America, and George Brown of Texas Instruments *(currently assigned to SEMATECH).*

The success of the conference is the result of both the hard work of many people in the industry who participated as coordinators, and the support of the Officers of Committee F-1. George Brown and Dinesh Gupta presided at the technical sessions and Howard Huff of SEMATECH joined Dinesh Gupta and George Brown in moderating the Panel discussions.

We are also thankful to all the presenters at the technical sessions who also joined as panel members. Many scientists from all over the world reviewed the manuscripts published in this book. Without their support, this publication would not have been possible. And finally, we acknowledge the hard work and efforts of the staff at ASTM in bringing the book to print.

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A Note of Appreciation

The quality of the papers that appear in this publication reflects not only the obvious efforts of the authors, but also the unheralded, though essential, work of the reviewers. On behalf of ASTM, we acknowledge with appreciation their dedication to high professional standards and their contribution of time and effort.

Dinesh Gupta
George Brown

Overview

The papers in this volume were presented at the conference on Gate Dielectric Integrity (GDI) held in January 1999 in San Jose, California to describe the concepts and metrology of the Gate Dielectric Integrity and discuss its applications for the material and device process and tool qualification. ASTM Committee F-1 on Electronics sponsored the conference. In addition to the technical presentations, a panel discussion was also held at the conference. A summary of the panel discussion is provided in Appendix 2.

A wide variety of topics relating to the subject of GDI are presented in this publication. These topics include concepts, methods, protocols, and reliability assessment as related to dielectric integrity. The characterization of thin dielectrics, various GDI measurement techniques, and discussion of important effects on the characterization of GDI is also included.

The proceedings section is divided as follows:

- Concepts
- Thin Gate Dielectrics
- Characterization and Applications
- Standardization and Round Robins—included as Appendix 1

Integrity of thin dielectrics in MOS devices is a dominant factor in determining the overall reliability of microcircuits. Even though many factors influence the final performance of a circuit, device reliability, in general, starts with high quality of silicon material. Thus, gate dielectric integrity measurements are one amongst several most commonly used within so-called "Wafer Level Reliability Tests". The dielectric layer is put under stress until it fails. This failure occurs in two phases: 1) a wearout phase in which the external stress slowly degrades the oxide, and 2) a breakdown phase where certain physical parameters are exceeded and the dielectric undergoes a runaway current flow. This high current flow causes the dielectric, shortly after the electrical breakdown, to break down thermally and to be permanently damaged. Dielectric reliability may be evaluated by forcing either current or voltage, either with a fixed level or ramped (stepped) stress. MOS capacitors with polysilicon gates are customarily used as testing devices. Two stressing methods are used: 1) time-zero dielectric breakdown (TZDB), and 2) time-dependent dielectric breakdown (TDDB).

In TZDB testing, the test structure is checked for integrity by measuring the sample response after applying a constant, initial voltage or current. The stress, either voltage or current, is then increased in steps until a defined failure criterion occurs, or the applied stress reaches a specified limit. In TDDB testing, on the other hand, after a similar initial test, a constant stress level, either voltage or current, is applied until a pre-determined failure condition or upper time limit is reached.

Professor David Dumin of Clemson University explores several oxide reliability assessment attributes and associates them with oxide integrity. He discusses oxide wearout and breakdown in terms of trap generation inside the oxide and locally high current regions occurring during breakdown events. He also presents a technique to characterize electric breakdown distributions. The latter are important in determining yield and early failures of the devices.

John Suehle of National Institute of Standards and Technology discusses the oxide reliability and GDI characterization for thin gate dielectrics. The value of Q_{bd} in case of thin dielectrics and its dependence on device area and current density is discussed in his paper.

Alvin Strong of IBM Microelectronics describes the advantages and challenges of a voltage step stress technique for TDDB measurements on oxides in the range of 10 nm. He proposes the advantages as being: 1) sample homogenization, and 2) sample size minimization. "The challenge may be in the interpretation of the data obtained from this technique sometimes, but the benefits outweigh this disadvantage," he says.

Bersuker and Werking of SEMATECH propose a model that provides a physical explanation for the electric field and oxide thickness dependence of charge-to-breakdown measurements. They note that relatively lower damage in thinner oxides, as determined by the concentration of generated traps, may produce a greater effect on oxide leakage current. Therefore, gate leakage current may not directly represent oxide damage after heavy stress. In fact, they find that after heavy stress, leakage current is determined by the probability of trap assisted tunneling, while in lightly damaged oxides the density of generated traps controls leakage.

Gilbert Gruber and Robert Hillard of Solid State Measurements, Marshall Wilson and Jacek Lagowski of Semiconductor Diagnostics, and Mark Dexter, et al. of Texas Instruments describe various non-contact measurements of Gate Dielectric Integrity, and discuss some of the applications of these measurements. Gruber and Hillard stress the need for making the measurements rapidly and accurately, and present the use of Hg probe for GDI measurements. They discuss the application of this measurement in monitoring a variety of process induced defects. Wilson and Lagowski describe COCOS metrology which maps contact potential difference and surface photovoltage produced from the application of electric charge on the dielectric surface. They discuss various applications of this technique in the monitoring of process flows and contamination. Hasslinger and Dexter utilize measurements made on the Quantox tool to monitor oxidation furnaces routinely, and to solve the problem of contamination introduced during a high temperature device process. This contamination had resulted in parametric failures in LOCOS devices.

The paper by Michael Seacrist describes various applications of GDI measurements in silicon wafer manufacturing. "Silicon wafer related GDI sensitivity has driven silicon wafer suppliers to reduce and eliminate the vacancy-related defects," he says and discusses other wafer properties such as the smoothness and purity of the silicon surface, which influence thin dielectric GDI measurements. The paper by Grann et al. of Wacker Siltronic gives GOI measurements at different oxide thicknesses.

Miner et al. of Applied Materials discuss the process and equipment technologies for depositing thin gate dielectrics. They also discuss the differences in the reaction chemistry of deposition responsible for improvement in gate dielectric integrity. Murakami et al. from Mitsubishi Materials Silicon Corporation apply the high-resolution GDI measurements to study the defect level in various types of silicon wafers such as, Pure Silicon™, epitaxial silicon, hydrogen annealed bulk silicon, so-called low COP silicon, and conventional CZ silicon wafers. Using the TDDB technique, they show a correlation between grown-in crystalline defects and defects in the deposited oxide.

The papers by Dumin, Suehle, and most others give a broad bibliography on the topic of gate dielectric integrity. The articles published in the 1999 Symposium on VLSI Technology may also be interesting to readers.

Appendix 1 gives the interim results of two round robins on the gate dielectric integrity. These round robins are currently in progress. One of the round robins is being conducted in the USA under the joint auspices of JEDEC and ASTM Committees, and the other in Japan under the joint cooperation of JEIDA and SEMI Japan Committees. The U.S. round robin is based on three test procedures: voltage ramp test, current ramp test, and bounded current ramp test. On the other hand, the purpose of the Japan round robin is to standardize the characteristic evaluation of silicon wafer quality by oxide dielectric breakdown method.

Finally, appendix 2 gives a synopsis of panel discussions held at the conference. The Panel members were the presenters of the papers included in this volume.

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