FATIGUE OF *Electronic Materials*

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EDITORS

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Peer Review Policy

Each paper published in this volume was evaluated by three peer reviewers. The authors addressed all of the reviewers' comments to the satisfaction of both the technical editor(s) and the ASTM Committee on Publications.

The quality of the papers in this publication reflects not only the obvious efforts of the authors and the technical editor(s), but also the work of these peer reviewers. The ASTM Committee on Publications acknowledges with appreciation their dedication and contribution to time and effort on behalf of ASTM.

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Foreword

This publication, *Fatigue of Electronic Materials,* contains papers presented at the symposium of the same name held in Atlanta, Georgia on 17 May 1993. The symposium was sponsored by Committee E-8 on Fatigue and Fracture. Scott A. Schroeder and M. R. Mitchell, both of Rockwell International Science Center, Thousand Oaks, California, served as co-chairmen of the symposium.

Contents

Overview

The first electronic systems developed consisted of circuit components attached to printed circuit boards by mechanical methods. Component leads were either placed through holes in the circuit board, twisted together, or secured with fasteners before soldering. The solder existed only to provide additional electrical and thermal conductivity to the system. Due to the relatively secure methods of component attachment, failure or small cracks in the solder rarely caused electrical system failure. However, relatively recent advances in circuit technology and the need to increase the density of electronic systems have reduced greatly the use of mechanical interconnections. In advanced soldering techniques such as surface mount technology (SMT), the solder is required to provide not only electrical and thermal connection, but mechanical integrity as well. The situation is further complicated by the power and environmental conditions placed upon today's electronic systems. Solder joints are commonly expected to provide an uninterrupted interconnection for several years at relatively high temperatures (0.5 to 0.8 T_m). Degradation of such joints under creep/fatigue conditions has increasingly become a major concern for the electronics community. Failure or even intermittent loss of conductivity in a single solder joint often reduces an entire electronic assembly to an inoperative state.

Considerable research, development, and design-related engineering activity has recently been undertaken by the microelectronics industry to address this problem. This effort has historically been product driven, resulting in material data and test methodologies designed to address specific operating environments and electrical systems configurations. In addition, test methods commonly employed are often developed without a detailed knowledge of mechanics or material science. Current research has roughly grown into three areas: (1) bulk material testing, (2) simulated solder joints, and (3) component testing. Among these areas, methodologies vary widely. Fatigue studies of solder have been undertaken using many different methods, including thin-walled tubes in shear, bulk tension specimens, lap shear joints, and simulated joints in shear. Test parameters such as strain rates, frequency in load control, stress-strain measurement methods, hold times, and thermal/mechanical fatigue effects are equally as varied. The situation for fatigue and reliability testing of entire components is even more complicated due to the variety of proprietary component geometries, operating environments, and in-house mechanical testing expertise. The currently existing database and test methodology is perceived as too complex, difficult to implement and extend to other situations, and is often developed without using existing mechanical testing expertise.

The purpose of the ASTM Symposium on Fatigue of Electronic Materials, the first on this topic, was to assemble a cross section of fatigue practitioners active in the microelectronics area to assess the current state and direction of fatigue/reliability research. A major long-term goal of this symposium and subcommittee activity is to provide a forum for fatigue researchers from a broad spectrum of disciplines and backgrounds within the microelectronics industry to compare and evaluate fatigue test methodologies for eventual development of testing guidelines. Such collaboration has the obvious benefits of providing an industry-wide source for future refinement of fatigue testing methods for electronics and for providing the basis for a more widely applicable database of solder and other electronic material properties.

The first five papers in this STP provide valuable insight into the various methods in use to characterize the fatigue/creep interactions present within solder under typical temperature and loading ranges of electronic systems. These methods incorporate differing experimental and analytical techniques, highlighting the diversity in methods used to analyze fatigue/creep in small components at high homologous temperatures. Within this diversity also exist common approaches for performing fatigue studies where creep, temperature, and hold time effects are prevalent.

The next two papers further detail the complexity of fatigue/reliability testing of electronic component systems. "Test Methodologies to Perform Valid Accelerated Thermomechanical Fatigue Tests of Solder Joints" by D. Frear, N. Sorensen, and J. Martens is an excellent overview of the inherent complexities in accelerated fatigue testing of materials subject to high homologous temperatures and continual microstructural changes. The second paper, A study of the high-cycle fatigue of Kovar, demonstrates that while the focus of fatigue in microelectronics is often on solder alloys, electronic components are complex systems subject to fatigue of various subsystems. The paper by Frear et al. received the "Best Paper" award for this symposium.

The final two papers provide examples of fatigue and creep characterization applied to reliability assessments of actual electronic components. While considerable progress is evident in this area, there remain a number of unresolved issues to consider before truly general, sufficiently detailed design and analysis approaches are available.

The symposium chairmen gratefully acknowledge the authors and reviewers of the manuscripts. Their participation, as well as that of the ASTM staff, has made this publication possible. It is hoped that the subject matter of this symposium will generate cross-disciplinary interest and stimulate cooperative efforts among the organizations active in solder/electronic material research, leading to a forum for test guideline formation.

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