APPENDIX I

PANEL DISCUSSIONS ON COOPERATIVE RESEARCH: A SYNOPSIS

(The material presented in this appendix is based on the best recollections of editor. The material did not go through the review process and is presented for information only.)

The panel was comprised of Erich Bloch, Chairman, Semiconductor Research Cooperative (SRC) and Director, National Science Foundation; Richard Fair, Vice President, Microelectronics Center of North Carolina (MCNC); Angel Jordan, Provost, Carnegie-Mellon University; James Meindl, Director, Stanford Center for Integrated Systems (CIS); and William Oldham, Professor, University of California, Berkeley with Dr. Jordan being the moderator. After brief presentations on the activities of various organizations on cooperative research, discussions and questions from the audience followed. The summary of the presentations and responses to questions is presented below.

SCOPE AND PROGRAMS OF SEMICONDUCTOR RESEARCH COOPERATIVE: ERICH BLOCH

The Semiconductor Research Cooperative was set up to provide a clearer view of limits, directions, opportunities and problems in semiconductor technology; to decrease fragmentation and control redundancy in semiconductor research; to establish efforts for above-threshold research in critical areas that may be beyond the resources of many companies individually; to enhance image of the industry in order to attract more talents; to enhance university-industry ties; and to provide scientific and technical information base for industrial development efforts. The elements of SRC projects include individual awards to universities and professors based on innovative research concepts; setting up of university research centers based on capability, negotiation and evolution; formation of the lead centers for the development of the evolutionary concept of shared complimentary research, facilities, management and administration; and the fulfillment, both by solicited and unsolicited proposals, of the research programs in the areas generated by the need and opportunity.

Specific projects have been undertaken in the three broad areas, namely; the microstructure technology

including the materials, phenonmenon, device physics, microscience and device fabrication; system & design including the design automation and system-component interactions; and production & engineering including the reliability, quality, packaging, manufacturing, assurance and testing. This type of research has been very well taken and is becoming an increasing concept with 50 different programs including 30 through the universities, presently in existence.

OBJECTIVES OF MICROELECTRONICS CENTER OF NORTH CAROLINA: RICHARD FAIR

The Microelectronics Center of North Carolina, established as a non-profit corporation in July 1980, is an interesting concept. It was set up with extensive research resources to provide a center for the coherent integrated programs for the satellite institutions namely; the University of North Carolina at Chapel Hill, University of North Carolina at Charlotte, North Carolina State University, Duke University, North Carolina A&T State University and the Research Triangle Institute.

Present programs include the equipment, fabrication, computer and communication technologies with teaching laboratories. The objective of vertical integration for research and development is carried out through the interaction of university centers and industrial affiliates in the research, both basic and applied; the process and equipment technology; and production including the design and manufacturing from mask to circuits (Fig. 1).

The Microelectronics Center is working its way to its long-range objective of establishing a nationally-competitive technological environment.

COOPERATIVE RESEARCH - UNIVERSITY POINT-OF-VIEW: JAMES MEINDL

The research conducted at the university is supported financially either by the institution itself, state government, federal government or the private industry either individually or a group of corporations joined together through programs. The key issues to the joint corporate sponsorship of university research are the promise, problems, assessment and the strategy.

There is a promise for the university in achieving advancements to the graduate students, staff and the

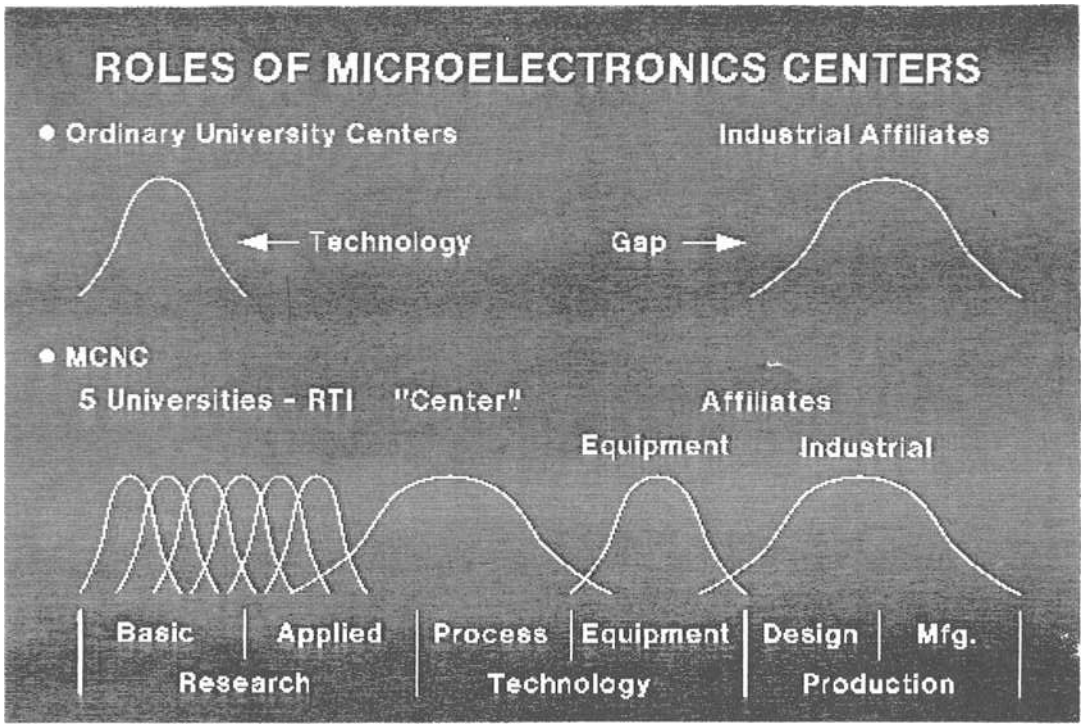
ROLES OF MICROELECTRONICS CENTERS
• Ordinary University Centers
Industrial Affiliates
Technology
Gap
• MCNC
5 Universities - RTI "Center"
Affiliates
Equipment
Industrial
Basic
Applied
Process
Equipment
Design
Mfg.
Research
Technology
Production

FIGURE 1

faculty, and the renovation of the equipment and a promise for the industry in having more graduates available and getting the research done in academic environment. The problems arise because of the restrictions to publications, owership of patents and copyrights, tendency to emphasize development rather than research, deemphasis of arts and humanities and the control on research areas and professorships, threatening the academic freedom.

Cooperative research is applauded from the humanitarian point-of-view because it provides an efficient use of human intelligence to improve the quality of life of all people; from the national point-of-view, it stimulates innovation and improves productivity and quality; and from the corporate point-of-view, it provides a competitive edge and an advantage to cut down the lead time.

And strategically, cooperative research provides a consensus for achieving leadership in technological innovation and production through the joint efforts of government, industry and academia.

THE UNIVERSITY RESEARCH - A PHILOSOPHICAL VIEW: WILLIAM OLDHAM

Industry plays an important role in university research because it brings relevant topics. It is more interesting for students and staff to involve in this kind of research because of its immediate applications. Modern research is done by a team of people who cooperate with each other and bring in new ideas or strenghten an idea by developing it. Excellent research is being conducted overseas, both in industry and university, some of which is government-sponsored. There is a need for better international cooperation and technical exchange.

Technical conferences provide good exchange media. They are inspirational.

GENERAL COMMENTS - ANGEL JORDAN

Competitiveness, quality and productivity are very much in place at this point, specially in the semiconductor industry. Erich must be commended for taking the lead in the idea of cooperative research. Bill's comments are excellent. In University, we are teachers first. We also do research. The main role is to educate, write books and teach with the current

technology. Research is, of course, essential and keeps us abreast with the state-of-the-art.

COMMENT: (Person from audience, unidentified) Industry helps a student understanding the practical problems. If students had one or two jobs before they went for higher studies, they would, probably, get better grades and get experience faster.

QUESTION: (R.I.Scace, National Bureau of Standards) Regarding the SRC programs, what comments do you have on the effects and results of the cooperative research, specifically in relation to the measurements?

RESPONSE: (Fair) As far as MCNC is concerned, SRC programs are very important. SRC funding is better, rather than the federal funding.

(Meindl) Universities gain from SRC projects because interaction with technical persons in industry is important. Further, SRC projects involve applied research which Oldham called as relevant research.

(Oldham) It is better for the professors to get involved in the complete projects which SRC awards. It takes too much time otherwise, for the professors to gather up money for the smaller projects.

(Bloch) The SRC programs may be measured in two ways (i) qualitative aspects which include the interaction and exchange of information. These are easier to measure. (ii) quantitative measurements including enhancing and enlarging the semiconductor industry, more graduates and more publications and patents. This aspect is not easy to measure.

QUESTION: (D.Sheldon, Roberts Consultants) (i) If the persons in industry want to go back to universities, they find resistance from the academic people, and also find that their salaries in the academic field will not be compatable with what they get in industry. How can this be simplified?

(ii) Percentage of graduate students is decreasing. How can we change this trend?

RESPONSE: (Fair) Special positions at special salaries are sometimes created with payment of exorbant salaries that upsets people. It is my experience that people, in a short time, adjust themselves in the new environment.

(Jordan) Salary is not really a problem. The real issue is the equipment and facilities needed to create first class research, the cost of which is increasing. That is where SRC could bring in new innovations.

QUESTION: (W.R.Bottoms, Varian Associates) I see two problems in cooperative research (i) the Sherman act, and (ii) everyone likes to have an advantage over the other. How do you see the cooperative research with these points in mind?

RESPONSE: (Bloch) There is no problem legally. In cooperative research, university is benefited because of publications. Present anti-trust laws are being looked into These laws are subject to interpretation.The country needs to be developed as a whole. There will, probably, be a bill in Congress soon which will make cooperative research implementation easier. In development area, however, SRC has a problem e.g., it is definitely difficult for 20 companies to get together and develop a product.

QUESTION: (M. Pawlik, GEC Research, Wembley, U.K.) In England, Japan and many other countries, governments participate in funding for the development of an industry by setting up 'National Programs'. U.S. does not have these programs. Are we doing something wrong in Europe and Japan?

RESPONSE: (Meindl) There is a lead program funded by U.S. government. The question is whether there should be a national program in microelectronics. My answer is no. The resources will be further depleted if such a program was set up. Rather than setting up national programs, U.S. government

support should be provided to the existing cooperative organizations.

QUESTION: (K.E.Benson, AT&T Bell Laboratories) How about the technologies other than microelectronics? Those are important as well.

RESPONSE: (Jordan) There are many other industries which are getting exposure in research such as, steel, manufacturing, robotics, etc. through research grants to universities. Transportation has had some difficulties. It is the high tech area which, being glamourous, gets little more attention.

(Fair) Energy field is very active and is being well-funded.

QUESTION: (A.R.Blew, Lehighton Electronics) How SRC programs involve in the development of products that can be sold?

RESPONSE: (Bloch) Universities do not necessarily want to finish the product. It might happen accidently. It is the generic or basic research and understanding the fundamentals which is more important and not the actual design. The cooperative programs have been extended to include design automation. That is as far as we should go, otherwise both sides, the university and the industry, will be disappointed.

Dinesh C. Gupta
Symposium Chairman and Editor

APPENDIX II

WORKSHOP SESSIONS

The material presented in this appendix has been written by editor and is based on the best recollections of editor and chairmen of the workshop sessions. The material did not go through the review process and is presented for information only.

1. CONTROL OF CONTAMINANTS
(Chairmen:A.Rapa & W.R.Schevey)

In semiconductor industry, control of contaminants was most important, both for the functional yields and the reliability of the devices. Semiconductor devices were very sensitive to particulate contamination during manufacture. Discussions in the workshop session took place on the increase in the degree of sensitivity as device features shrank and circuit densities increased. It was pointed that the power devices were as sensitive to contamination as the VLSIs.

Major sources of particulate contamination were discussed. One major source of contamination was the human body which, when came in contact with the room air released particles. There was discussion on various classes of clean rooms, especially the class 10 or lower where there were monitoring problems and also, the problems of definition. Even the tiny particles, 1000 angstroms or less affected the performance and reliability of a circuit or a device. It was pointed out that ASTM was working on solving these problems through consensus and better test procedures.

Other sources of contamination were the water chemicals, gases, plastics and photochemicals. Outgassing of plastics was discussed by Rapa in detail. Because this contamination was chemical in nature, very small (<100 angstroms) particles affected the devices, specially the ones fabricated on the MOS process. Two types of chemicals, namely; MOS and VLSI grades were discussed. Stripping and wet cleaning cycles comprising of HF cleans, dump rinse, spin dry or the blow dry contributed to large contaminations unless there was special care taken at each step to use sub-micron filters. Question was whether automation would solve the contamination problem. The reply was no, not by itself. The answer to contamination control was in a well-designed care at each and every fabrication step.

2. INTERCONNECTION TECHNOLOGY
(Chairmen:P.Douglas & G.G.Harman)

As integrated circuits continued to increase in density and sophistication, the requirements on interconnections became more demanding and the field, traditionally rather dull and labor intensive, became exciting with significant advances in automation. Thedesirability of automation in wire bonding was noted for its consistent quality as well as its speed. High speed ball bonding was discussed in detail. It was pointed that the wire bond consistency, which resulted in higher yields and more reliable circuits, and increased throughputs, and which helped to control production costs, were the main motivations in this field. As with most other semiconductor fabrication operations, the quicker wire bonding was done, the lower was the cost of production. It was noted that the speed of present-day bonders could still be increased. Mechanical motion restrictions on momentum transfer, vibration frequencies and wire-handling were the main considerations in increasing the speeds from today's capability of seven-to-eight wires per second to ten-to-twelve wires per second. Slowing down the speed of each head and operating with multi-head bonders was mentioned to be another solution towards high throughputs.

A requirement for ball bonding was the formation of a perfect ball. Its surface had to be free from oxides and other contaminant layers which were detrimental to the adhesion of the ball to the substrate. Discussions took place on ball bonding using the nonprecious metals such as Al, Mg and Cu. The ball formations on Al-alloy wires were hindered by oxide layers which were already present on the wire surfaces or which were formed when wires were heated in air. The ball formations and the mechanical properties of Al-1% Si, Al-1% Mg and Al-1/2% Mg bonding wires were presented. Discussions were held on the intermetallic formations (so-called "plagues") and the solutions to eliminate them were presented.

The ball bond shear testing was the topic of detailed discussions at the workshop. Shear testing was performed by pushing the edge of the bond and measuring the force required to make it shear from the bonding pad metallization. According to Harman of the National Bureau of Standards, shear testing was the most accurate method of evaluating the ball bond quality today. It was pointed that it was a good

practice to observe the entire test through a microscope, being ready to lift the shear tool at the point of failure. This action minimized the over-travel of the tool which could damage another portion of the device. Shear test could not be performed on wedge bonds due to wedge bond's low profile. Techniques for on-line production testing were presented by Charles et al of The Johns Hopkins University.

New applications of tape bonding and bumped tape processing were briefly discussed. And the activities of ASTM Subcommittee F1.07 on Interconnections were described.

Dinesh C. Gupta
Symposium Chairman and Editor

APPENDIX III

PANEL DISCUSSIONS

The material presented in this appendix has been written by W. Murray Bullis for Material & Process-Induced Defects and by Dinesh C. Gupta for Ion Implantation and Advanced Lithographic Technology. It is based on their best recollections. The material did not go through the review process and is presented for information only.

1. MATERIAL AND PROCESS INDUCED DEFECTS

The panel was comprised of the following panel members: L.Jastrebzski, RCA Laboratories; J.Lagoski, Massachusetts Institute of Technology; J.H.Matlock, SEH America; J.R.Monkowski, Pennsylvania State University; and C.J.Varker, Motorola Incorporated. W.Murray Bullis, Siltec Corporation was the moderator.

This session was intended to provide additional time for general discussion of the topics such as, intrinsic and extrinsic gettering, denuded zone formation, oxygen precipitates and effects on device characteristics. In particular, to provide guidence to future activities in ASTM Committee F-1, the session was concerned with the metrology of defects in silicon, the limitations of available techniques, and the effects of these limitations on the interpretation of physical phenomema.

The session opened with a late-news paper presented by T.Abe of the SEH R&D Center on the behavior of oxygen in the silicon melt. He concentrated his comments on the amounts of oxygen incorporated into heavily doped antimony substrates. Oxygen and other impurity distributions were obtained using a CAMECA ims-3f with an improved sensitivity, because standard FTIR absorption methods can not be used for oxygen measurements on heavily doped substrates. Previously it had been noted that there is a difference in oxygen precipitation between crystals doped with boron and those heavily doped with antimony. Abe showed that the difference is due to lower oxygen in antimony substrates and not due to a fundamentally different mechanism. The lower oxygen concentration is caused by oxygen evaporation during growth from the heavily doped antimony melt.

This was followed by opening statements by each of the

panelists in which they described their particular areas of activity and concern. These areas include: effects of oxide precipitates on electrical properties, with emphasis on MOS technologies; effects of different ambients on oxide precipitation and denuded zone width; effects of defects and thermal cycles on IC properties; and electronic properties of oxygen-related defects in silicon and gallium arsenide on a microscale. The final panelist raised the following questions for consideration:

> Are crystallographic defects assets or liabilities? What defects do we want in processed wafers? How is defect generation related to as-grown silicon characteristics? What should we measure? Precipitation rates? Defect density? Distribution of defects? Etc.

In addition, he emphasized the need for microscale studies of oxygen precipiation kinetics, the properties of different oxygen-related defect states, and the means to induce oxygen in a given state.

In the ensuing discussion, the following points were brought up. In keeping with the informal, off-the-record nature of the discussion, contributors are not identified.

CARRIER LIFETIME AND OXIDE PRECIPITATION

Results of measurements of generation (C-t) and recombination (reverse recovery) lifetimes were reported. The former relates to the carrier lifetime in the bulk. A correlation with precipitated oxygen was observed. Both quantities are important in predicting holding time; the highest generation lifetime does not mean the longest hold time unless the recombination lifetime is correct. From the ratio of these lifetimes one can infer the effectiveness of the denuded zone. Surface photovoltage also provides a measure of the denuded zone depth which is equal to the diffusion length determined from this technique. It was emphasized that there is a finite density of oxide precipitates at the surface, even where there is an apparent denuded zone. A precipitate density of 100 cm just under the surface is adequate for CMOS circuits but too large for CCDs. A good method for counting such small defect densities is needed. It was emphasized that small precipiates which may not result in etch pits can exist in the denuded zone. In addition, it was observed that preferential etching of

oxide precipitates does not yield unique etch figures and that positive identification of an etch pit with a precipitate must be made by independent means.

MECHANICAL STRENGTH

A question was raised regarding the state of oxygen in silicon which leads to increased mechanical strength and resistance to warp. Conventional wisdom holds that it is oxygen in the interstitial form; it is widely observed that an increased oxide precipitate density leads to an increased propensity for a wafer to warp. Some hold that it is a non-interstitial form of oxygen which affects mechanical strength; however, no means has yet been devised to uncouple this form from the interstitial form so the question cannot be fully resolved. Later in the discussion, it was observed that nitrogen concentrations some three orders of magnitude lower than the usual interstitial oxygen concentration in crucible-grown silicon provide similar mechanical characteristics.

HAZE AND GETTERING EFFICIENCY

A request was made for definitive information on the relationship between haze and metallic contamination. It was observed that silicon from some sources shows haze while other silicon does not appear to. A suggestion was made that the silicon interstitial may be the key point defect in forming haze. Without reaching a real answer on the nature of relationship, the discussion moved to a more general consideration of contamination and gettering. Metallic contamination has been unambiguously linked to device failure. There was some concern about extrapolating results from intentionally contaminated wafers to the much lower contamination levels likely to be found in device lines. Although the concentration of metallic contaminants at the surface may be as high as $10^{17} cm^{-3}$ it was asserted that levels several orders of magnitude lower are required for VLSI processing. Except for data obtained in connection with solar cell development, no direct data to show what is being improved by gettering seems to be available. Further, data regarding the efficiency of various types of defects for gettering different metallic contaminants is needed. There is evidence that some stacking faults are more effective gettering sites than others. There is also some evidence that wafers with slower precipitation rates have more efficient gettering than rapidly precipitating wafers. A correlation has been

shown between fast precipitation and a significant concentration of non-interstitial oxygen in the as-grown wafer, but the correlation with carbon content is tenous at best.

In summary, many experiments have been carried out, and much data has been analyzed. Many believe that enough understanding has been gained to permit effective materials engineering to be achieved at least under certain conditions. Nevertheless, there appear to remain many questions for which definitive answers are still elusive. Much additional understanding of defect interactions and characteristics on a microscale must be developed to provide these answers and put materials engineering for VLSI on a solid basis.

W. Murray Bullis
Siltec Corporation
Mountain View, California
Panel Moderator

2. ION IMPLANTATION

The panel on Ion Implantation consisting of P.Byrne, LSI Logic; B.Kirby, National Semiconductor Corporation; C.McKenna, Varian Associates; G.Norton, National Electrostatic Corporation; and G. Srinivasan, IBM Corporation was moderated by M.I.Current, Trilogy Systems Corporation and B.J.Masters, IBM Corporation. There were extended discussions on various topics including some on which the oral technical presentation were made in the morning session.

The moderators in their introductions mentioned that ion implantation had proved itself as one of the most important technologies in the fabrication of all kinds of semiconductor devices and circuits including the complex VLSIs. The applications are emerging in all phases of device processing, such as, gettering, threshold adjusts, source-to-drain dopings, buried layers, isolation islands, interconnects etc. The wide variety of applications have imposed stringent requirements on the implantation equipment. Equipment suppliers are finding hard to keep up with the growing technology.

Discussions started out on the effects of planar channeling in bipolar transistors resulting in large variations in gain across the wafer. The base was

shallow and was formed by using the implants in these transistors. It was mentioned that most of the effects of planar channeling could be reduced by orienting the wafer off axis from the ion beam during the base implant. The measurement techniques were discussed in detail, especially for the low-dose implants. The spreading resistance techniques were described by Ehrstein, Pawlik, Gruber and Mazur. The thin layer spreading resistance testing required the use of low penetration probe tips and shallow angles on the leveled specimens. Probe conditioning, angle measurements and specimen preparation were important in order to provide reproducible surfaces and sharp bevel edges. There were still some differences in spreading resistance measurements as compared to measurements made by analytical techniques, such as, Secondary Ion Mass Spectroscopy (SIMS) and Neutron Depth Profiling (NDP). Possible explanations for these differences were discussed.

There was lot of interest in the audience on the charging effects, effects of thermal annealing and the generation of defects in semiconductor surfaces. It was mentioned that there were two types of defect structures arising from ion implantations. One, which produced a heavily damaged single crystalline layer and the other which produced an amorphous skin layer on the silicon wafer. The former was the characteristics of lower doses and lighter implanted atoms and the latter was the result of high dose implants and heavier implanted atoms. Cooling during the implantation was also important, for example the lower wafer temperatures produced amorphous layers and higher wafer temperatures produced single crystalline layers. For high energy and high current implant, a thin crystalline film occurs over an amorphous layer. Thermal annealing at temperatures greater than 1000 C usually dissoluted the single crystalline defects and low temperature anneals, typically performed at 550 C, helped in recrystallizing the amorphous layer. Isothermal or heat pulse annealings must be carefully used as these tended to create strains along certain orientation planes in the wafer. The combination of radiation with thermal annealings, resulted in a faster transformation of amorphous layers to crystalline layers. It also stabilized the amorphous layer underneath the crystalline layer for high energy, high current implants.

It was mentioned that arsenic clustering may be important for understanding the distributions obtained

after high dose arsenic implants. Arsenic diffusions for these implants did not depend only on the interaction of arsenic atoms and charged vacancies but also on the clustering effect. The latter occurs due to the discrepancy between the number of carriers and the number of arsenic atoms at high arsenic doping concentrations.

Wafer charging models were discussed by C. McKenna and contaminations during the high current implants by T. Smith and G. Gruber. Fahrner amplified on his presentation of high energy implants. These implants were performed at the energies of 20 to 540 MeV. This technique was used to implant B,C,O,Ne,Kr and Ar ions in silicon, germanium and III-V compounds and some insulators. One of the applications of these implants was the improvement in turn-off times of thyristors.

3. ADVANCED LITHOGRAPHIC TECHNOLOGY

The panel on Advanced Lithographic Technology was formed of equipment and chemical manufacturers and the process technologists as the users of the systems to provide an interesting and informative dialogue. The panel moderated by P.L.Castro, Hewlett-Packard Laboratories and A.R.Neureuther, University of California, Berkeley included D.Alles, AT&T Bell Laboratories; B.Doyle, Varian Associates; G.A.Gerrettson, Hewlett-Packard Laboratories; J.S.Greeneich, Electron Beam Corporation; R.Martin, Shipley Company; R.F.W.Pease, Stanford University; D.L.Peltzer, Trilogy Systems Corporation, M.P.H.Shearer, JOEL USA; C.H.Ting, Intel Corporation; and J.Wiesner, Perkin-Elmer Corporation.

The discussion took place on advanced lithographic technologies including the x-ray, ion beam and e-beam systems, direct write systems, photo resist and source materials, technology and equipment trends. Much discussion centered on e-beam lithography and the use of e-beam for direct write systems. E-beam for mask making was mentioned by equipment manufacturers to be the well-established matured technology. Users of this technology differed with this view. According to Electron Beam Corporation, although big companies, such as, IBM and TI were already using in-house built direct-write e-beam systems in production environment, more than 90 percent of the use of e-beam systems was for mask making. At least two of the manufacturers, Varian Associates and Perkin-Elmer Corporation

mentioned that their e-beam systems could achieve overlay accuracy of about 0.1 micometers.

Registration accuracy, a 'must' in mask making is important but not so critical in lithographic application except in case of very complex circuits. Throughput in the direct write systems is, however, the main consideration which, with the moderate changes in the hardware, could be achieved. The throughput in e-beam direct write system is affected because one element is written at a time in series while in exposing a wafer using optical techniques, millions of elements are exposed at a time in parallel.

The users from the audience stated that e-beam for direct write was still used mainly in R&D laboratories. They questioned the manufacturer's definition of the throughput in terms of wafers per hour. Unless the throughput numbers included information such as, the size of the wafer and the complexity of the device in terms of feature size, density etc., it was very difficult to interpret the capability of a machine. Furthermore, the downtime of the machine was the key issue. These systems were very complex for the fabrication facilities to maintain them. Downtime which inherently included the time for the availability of parts and degree of the technician's training was a subjective term. It was suggested that if mean-time-between-failures (MTBF) was used, it would define the reliability of the machine in a conclusive manner.

There were discussions and comparisons of the optical and x-ray lithographic techniques, pointing to the diffraction and, therefore, the resolution of the optical lithography which x-ray techniques did not have. Even though x-ray equipments were still in development stage, they showed a promise in simplicity and, therefore, must result in greater uptime and more productivity.

As the new lithographic techniques evolve into manufacturing, the need for high resolution lithographic materials is increasing. Although resist considerations were not discussed in detail, the mention was made for the need for specifying the resist parameters more clearly. The important parameters such as, processing and development parameters including the preexposure and postexposure conditions, the sensitivity and contrast data, etch

resistance and the stability all affect the fabrication of the device in terms of yields.

A mention was made that the June 1984 issue of Solid State Technology will be carrying in-depth papers on the Resist Technology.

Dinesh C. Gupta
Symposium Chairman and Editor