Appendix 1

Interim Reports of Two Inter-Laboratory Round Robins on Gate Oxide Integrity, One Conducted by ASTM Committee F-1 and JEDEC Committee, And the Other Conducted by JEIDA Committee and SEMI, Japan

The two round robins, one conducted by ASTM Committee F-1 and IEEE-JEDEC Committee, and the other conducted by JEIDA Committee and SEMI in Japan are entirely different in their scopes. The ASTM/JEDEC round is being conducted in the USA to test gate oxide integrity with three test procedures, namely the voltage ramp, the current ramp and the bounded current ramp methods. The voltage ramp method is considered useful in determining changes in a given device process, and is supported by the ASTM Standard Test Method F1771-97[1]. The current ramp and bonded current ramp tests are supported by test methods published by JEDEC Committee[2]. John Suehle of NIST discusses the details of this round robin below.

The charge-to breakdown evaluation of a silicon wafer is widely used in determining the wafer quality for device yields and reliability. The purpose of the second round robin conducted by JEIDA Committee and SEMI Japan is to establish 1) the correlation between sample preparation conditions, measurement conditions, and 2) to compare the results of the oxide breakdown measurements performed on the multi-laboratory basis. Upon obtaining suitable conditions, it is anticipated that a method of measurement of silicon wafer quality in terms of oxide breakdown will emerge. This method will be useful by both the silicon producers as well as users who fabricate devices on the silicon wafers. Kikuo Yamabe of the University of Tsukuba discusses this round robin and provides initial results.

Both round robins are expected to be completed in the year 2000.

..... Dinesh C. Gupta, Co-Editor

Round Robin on GOI Test Methods Conducted by ASTM/JEDEC: Interim Report[3]

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The purpose of the inter-laboratory round robin is to evaluate the joint ASTM/JEDEC voltage ramp test procedure for ultra-thin oxides having a thickness down to 3 nm. The round–robin will also evaluate modifications made to the breakdown criteria used in the JEDEC current ramp and the bounded current ramp test. The failure (breakdown)

[1] ASTM Book of Standards, Volume 10.05. The test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F1.06 Section F on Metrology for Process Control, George Brown, Chairman.

[2] EIA/JEDEC Standard 35-1.

[3] Round Robin conducted by John Suehle of NIST and George Brown of SEMATECH (Texas Instruments Assignee).

criterion for the voltage ramp test was changed from an increase of 10 times in the measured current to a factor of 3 in the current-voltage slope change. The failure criterion for the current ramp was changed from a 15% drop in the measured voltage to a 5% drop in the measured voltage. The results from the round robin will be used to assess the robustness of the three breakdown tests when performed on different sets of equipment and to determine if any of the test parameters need to be modified

Texas Instruments, Inc supplied twenty wafers. The wafers were processed such that there were four sets of wafers having SiO_2 grown to a thickness of 20, 10, 5, and 3 nm. Sixteen wafers were patterned with round capacitor test structures with 4 different areas and four wafers were not patterned for Hg probing. Each participating laboratory is instructed to perform 3 tests: ASTM/JEDEC Voltage Ramp test, JEDEC Current Ramp test, and the JEDEC Bounded Current Ramp test.

Eleven laboratories have agreed to participate in the round-robin experiment. NIST serves as the reference laboratory. Three laboratories have completed the tests and three are currently conducting the experiment. Initial results indicate that the tests are robust and yield quantitatively similar reliability parameters even when performed on different test equipment. The round robin is expected to be completed in the year 2000.

Standardization of Silicon Wafer Evaluation by Oxide Breakdown---Results of first Round Robin conducted in Japan

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Higher operation speed and better reliability is required in modern silicon ULSI's and better yields and high reliability are necessary in order to ensure high device performance. It is known that the silicon substrate quality as measured by the defect density strongly influences the quality of silicon dioxide film. Further, it is known that 1) surface metallic contamination and 2) oxygen precipitates and voids influence the breakdown defect densities of thermally grown SiO_2 films deposited on silicon wafers. The voids are aggregates of the atomic vacancies in the silicon substrate[4-6]. The hydrogen-annealed silicon wafers or epitaxial silicon wafers generally have lower densities of oxygen precipitates and voids near the surface and, thus provide low oxide breakdown defect density. Both of these materials are, however, costlier than the CZ wafers. The evaluation of the silicon wafers by dielectric breakdown of thermally grown silicon oxide on silicon substrates is very sensitive and practical, but the results are affected by the sample preparation and measurement conditions. In the first round robin, the conditions of sample preparation and measurements employed by participants was checked.

[4] Yamabe, K., Taniguchi, K. and Matsushita, Y., Thickness dependence of dielectric breakdown failure of thermal SiO_2 films", *Proc. IRPS '83, IEEE*, 1983, pp. 148-190.

[5] Yamabe, K., Taniguchi, K., and Matsushita, Y. "Thickness dependence of dielectric breakdown failure of thermal SiO_2 films", *Defects in Silicon, The* Electrochemical Soc., 1983, p.639.

[6] Yamabe, K., and Taniguchi, K., "Time Dependent Dielectric Breakdown of Thin Thermally Grown SiO_2 Films", IEEE Trans. Electron Devices, ED-32, 1985, p.423

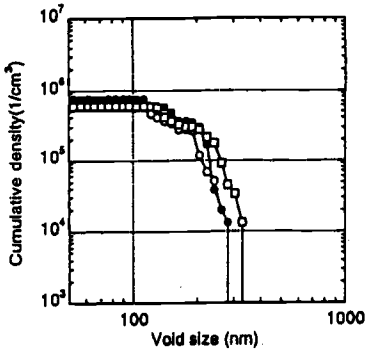

Fig.1. Grown-in defect density distribution by OPP.

The participants of the first round robin are 7 companies, MEMC Japan Ltd., Komatsu Electronic Metals Co. Ltd., Shin-Etsu Handotai Co. Ltd., Nippon Steel Corp., Toshiba Ceramics Co. Ltd., Wacker Chemicals East Asia Ltd., and Mitsubishi Material Silicon Co.

Samples were cut from one phosphorus-doped Czochralski-grown P-type (100)-oriented silicon crystal ingot with a resistivity 9-11 Ω. Cm and were identically processed. The interstitial oxygen concentration was $8\text{-}9\times10^{17}cm^{-3}$ (JEIDA standard). Three wafers were selected from the lot and the grown-in defect density distributions were determined by Optical Precipitate Profiler (OPP) measurements. It was confirmed that the total defect density was $6\text{-}8\times10^{5}$ cm^{-3} in all wafers chosen (Fig. 1).

Fabrication of MOS capacitors:
Two wafers were provided to each participant who fabricated MOS capacitors using the following method. Each company cleaned the wafers by their own cleaning method, deposited silicon oxide of 10 and 25 nm at 900°C in an atmosphere of pure dry oxygen, and deposited phosphorus-doped polysilicon films of 200-400 nm thickness and with a sheet resistance of less than 50 Ω/□ by LPCVD method. Lithography and either a chemical dry etching or wet etching technique and the company's own photomask was used to form the electrode pattern. The sizes of the capacitors' gate areas were 1 and 10 mm^2. Back surface contact was not employed.

Evaluation of dielectric breakdown[4, 5]
TZDB (Time zero dielectric breakdown) measurement condition: The gate field of the MOS capacitor was allowed to increase in steps of 0.25 MV/cm until the leakage current of the gate oxide exceeded the pre-determined dielectric breakdown current of 1 μA. The gate field at this time was made to be the dielectric breakdown electric field. The gate field was applied in the direction of the gate electron injection. No compensation was made for the flat band voltage Approximately 100 capacitors were measured for each condition, and histograms were drawn for three breakdown modes as follows:
A-mode - $E_{BD} \leqq$ 1MV/cm, B-mode - 1 MV/cm $< E_{BD} \leqq$ 8MV/cm, and C-mode - E_{BD} >8 MV/cm.

Results and discussion

Fig. 2 shows typical breakdown mode ratios and their average value. Each ratio was calculated for MOS capacitors fabricated by company B and measured by 7 participants. The gate oxide thickness was 25 nm and capacitor area was 10mm^2. Wafer #F1 measured by company F had lower B mode failure fraction by about 15 % in comparison to the

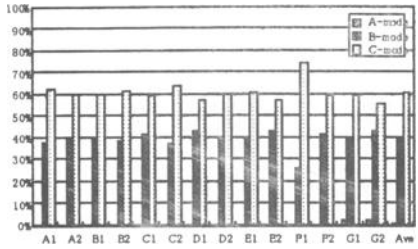

Fig.2. Oxide breakdown mode ratios measured by 7 companies.
Company B fabricated the MOS capacitors.

measurements made by other companies. This result could be explained, because the company F made an error in the measurement. Accordingly, the data of #F1 was excluded from the average calculation. Assuming that the oxide breakdown defects have the Poisson distribution, the oxide defect density, α_{ox}, may be calculated from the failure fractions in Fig.2, using equation 1.

$$\alpha_{ox} = - \ln (1-F)/S \qquad (1)$$

Where, S is the capacitor gate area, and F is the failure fraction for each oxide breakdown mode.

In Fig.3, the average defect densities for the MOS capacitors fabricated by 7 participants are shown. The defect density are low for companies B and D, high for companies E, F and G and in between these for companies A and B. The average density of the B mode defect is 5.8cm^{-2} with a dispersion of $\pm$ 1 cm^{-2}. The average A mode defect density is lower than 0.1cm^{-2}. The average oxide thickness is about 24.9nm. Assuming that the silicon thickness converted to the silicon dioxide is 0.44 times the oxide thickness, the converted silicon thickness is 11.0 nm. Considering the low A mode defect density, it is reasonable to presume that the B mode oxide defect can be mainly due to defects in silicon substrate. Therefore we can estimate that the defect density in the silicon substrate

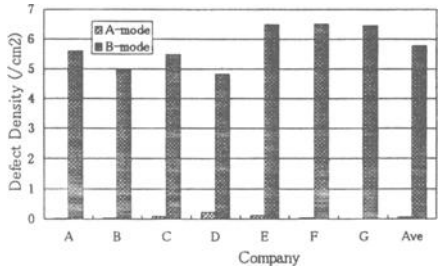

Fig. 3. Oxide breakdown mode ratios measured by 7 participants. MOS capacitors were fabricated by company B.

is $(5.3 \pm 0.9)\times10^{6}cm^{-3}$. As shown in Fig.1, the dispersion of the COP (Crystal Originated Pits) density of the silicon crystal ingot is $6\text{-}8\times10^{5}cm^{-3}$, which is about tenth of the electrically measured defect density described above. This difference may be explained as follows: First, the minute defects, which cannot be measured by the OPP technique, may become origins of the B-mode oxide defects. Secondly, there may be some defect origins during wafer process such as surface contamination after cleaning treatment and diffusion of phosphorus atoms near the polysilicon gate electrode at the oxide interface. However, considering that the dispersion of the B mode defect densities among the 7 fabricating companies is at most $\pm$ $1cm^{-2}$, the second reason can be omitted. The lower detection limit for defect diameter by OPP measurement is about 100nm. In Fig.1, the increasing trend with decreasing defect diameter is not perfectly saturated at 100nm. Defects of diameter less than 100nm, of course, exist in silicon. And it is hard to consider that the dielectric breakdown of 25nm oxide is not sensitive to defects in silicon with diameters of the order of ten nanometers. This explanation allows one to believe that the sensitivity of defect measurement by OPP method is lower than the defect evaluation by dielectric breakdown of the thermally grown silicon dioxide on silicon substrate. For the gate area of 1 mm^2, the measured capacitor number of 100 is too small to estimate the exact defect density.

Fig.4 shows defect densities of the 10nm oxides. Compared to defect densities in 25nm oxides, the defect densities of 10nm oxides are remarkably lower except for the company, D. Due to their fabrication process, companies D and F had higher defect densities.

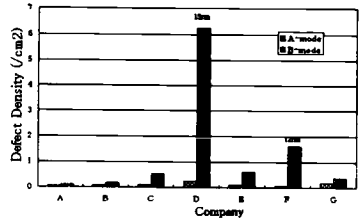

Fig. 4. A- and B-mode oxide defect densities for MOS capacitors fabricated by each participant. Oxide thickness is 10 nm.

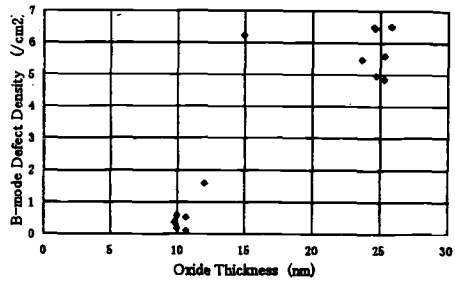

Fig. 5. B-mode oxide defect densities as a function of oxide thickness.

In Fig.5, the oxide defect density is plotted as a function of silicon oxide thickness. The defects are distributed uniformly with a density, ρ_{si}, in the vicinity of the silicon surface and become dielectric breakdown defects upon incorporation in the oxide by thermal oxidation. Assuming that all B mode defects come from defects in silicon substrate, α_{ox} of the B mode is given by

$$\alpha_{ox} = \rho_{si}\, T_{ox}/0.44 \qquad (2)$$

The B mode defect density should be in proportion to the oxide thickness, T_{ox}. However, in Fig.5, the oxide defect density steeply increases when oxide is thicker than 10nm, as explained by inverse relationship of oxide breakdown field and oxide thickness. Since the B mode failure fraction is too low, the same measurement for dielectric breakdown of the two oxides, 10nm and 20nm, is not suitable for the evaluation of defects in silicon wafers. In case of 10nm oxide, another evaluation method such as a time dependent dielectric breakdown (TDDB) is proposed.

Oxide thickness

The error in the value of oxide thickness affects the oxide breakdown mode ratio. The influence is especially large for oxides thinner than 20nm.

The leakage current of silicon oxide film depends upon the electric field across the oxide and, is controlled by the. Fowler-Nordheim (FN) tunneling mechanism. The leakage current in different oxide thickness will be equal if the series resistances in the oxides, coming from the silicon substrate, polysilicon electrode and wiring etc., are equal. Therefore, if the same measuring system is used, a variation in oxide thickness may be calculated from the gate voltage distribution that gives equal leakage currents for the capacitors with equal gate areas. From the current-voltage characteristics, gate voltages were obtained for a leakage current of 1×10^{-6} A/mm^2. Oxide thickness was measured on the test wafer by ellipsometric measurement. Figures 6(a) and 6(b) show the correlation between gate voltage and the oxide thickness for 25nm and 10nm oxides. In fig. 6(a), all data points are within a region enclosed between +10% and -10% lines, while in fig. 6(b), only one data point is below the -10% line. This indicates that the leakage current of the

oxide deposited by this company is higher than that of the leakage currents of oxides from other companies. A round robin for the oxide thickness measurement is planned among the seven companies.

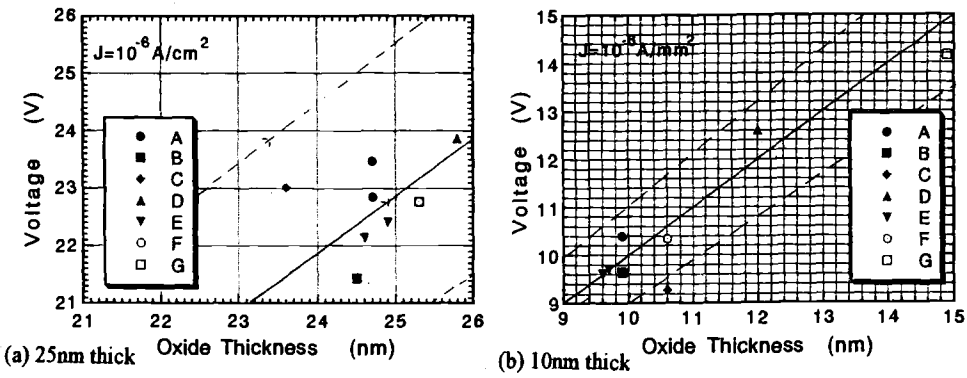

Fig. 6. Critical gate voltage vs. oxide thickness measured by ellisiometry. The critical gate voltage is a voltage at which the gate oxide leakage current reaches 10-6 A/cm2 of MOS capacitors with oxides of (a) 25 nm thick and (b) 10 nm thick

Conclusion

This round robin consisted of sample preparation and measurement of oxide breakdown by seven companies in the process of evaluating silicon substrate quality by gate oxide integrity. It is anticipated that following a second round robin, the standard test method for GOI measurement can be recommended in the year 2000

Appendix 2

Panel Discussions – A Synopsis

Dinesh Gupta and Howard Huff wrote the material presented in this appendix. It is based on their material and feedback from Dave Dumin, Gennadi Bersuker, Yoshio Murakami, and John Suehle. This material, however, did not go through the review process and is presented for information only.

The Panel members included G.Bersuker, SEMATECH; M.Dexter, Texas Instruments; D.J.Dumin, Clemson University; E.D.Grann, Wacker Siltronic; G.Gruber, Solid State Measurements; G.Miner, Applied Materials; Y.Murakami, Mitsubishi Materials Silicon Corporation; T.Pavelka, Semilab Rt; M.Seacrist, MEMC Electronic Materials; A. Strong, IBM; J.S.Suehle, NIST; and M.Wilson, Semiconductor Diagnostics.

Gate dielectric integrity (GDI) was described to be one of the most critical parameter of CMOS devices. Certain grown-in defects incorporated during crystal growth impact the integrity of the gate dielectric films. Thus, GDI has frequently been used to classify the quality of silicon wafers. These measurements have led silicon suppliers to develop crystal growing processes, which suppress the formation of point defect agglomerates, thus reducing or eliminating vacancy-related defects. GDI performance in wafers using these technologies can approach epitaxial wafer equivalence. It is, however, not well understood how much other wafer properties such as microroughness, surface contamination etc. will influence thin dielectric GDI. Continued scaling of gate dielectric thickness for smaller technology nodes raises reliability concerns for ultra-thin dielectrics because excessive leakage current and soft breakdown present new challenges.

Many methods are used to introduce the stress during measurement. These methods include constant voltage, constant current, and VRAMP or JRAMP (step or bounded). The ramped current and constant current measurements of Q_{bd} can only be correlated if test conditions are properly taken into account.

The results for thicker oxides (>10 nm) measured under constant voltage and. constant current stress are closely related. For thinner oxides ($\leq$ 3 nm, for example, where direct tunneling becomes more important) however, Q_{bd} measured by a constant current stress (CCS) is very sensitive to the stress conditions, and tends to lose its significance as a metric.

Published literature has shown that even for thicker oxides, Q_{bd} cannot be directly correlated with dielectric lifetime determined by device testing, but can be useful as a rapid process control method for determining dielectric defect density. Data is available

in the literature, however, which shows that if extrinsic defect density is the desired parameter, ramp test duration could be decreased from 25 sec down to one sec with no loss of resolution. Q_{bd} is not a predictor of dielectric lifetime, but it can be used to identify defective dielectrics.

The detection of the breakdown event during the breakdown test becomes quite difficult, especially in ultra-thin dielectric films. The event is noted in terms of a sudden decrease of current in the constant current method. According to one panel member, "soft- or quasi-breakdown may occur during testing of oxides thinner than 5 nm. Leakage was also a limiting factor in dielectric scaling. It was mentioned that the minimum thickness is 2.4 nm based on a defect generation model with a tolerable leakage current of 1 A/cm^2 was identified from reliability consideration [1].

The calculation of defect density is based on a Poisson distribution using the following relationship

$$Y = \exp(-AD), \qquad (1)$$

Where:
Y = yield of good units in terms of defined criterion,
A = area of sample, cm^2, and
D = defect density, defects/cm^2

The yield may be represented by *(1-F)* as follows:

$$1\text{-}F = \exp(-kt^n) \qquad (2)$$

Where, *k* and *n* are constants, characteristic of the transformation of a good to a bad device, *F* ($\neq$1) is the fraction of devices that fail, and *t* is the time. Equation (3) is used to convert the cumulative percentages to Weibull format (where *ln* is the natural log operator):

$$\ln\{-\ln(1\text{-}F)\} = +\ln k + n \ln t \qquad (3).$$

The Weibull distribution is often used to present Q_{bd} results. According to one panel member, "the CCS method is preferable from a material characterization point-of-view because CCS is not too sensitive to the variation in the oxide thickness." However, constant voltage stress (CVS) is preferred for thinner oxides. Electrode polarity has a large effect on Time Dependent Dielectric Breakdown (TDDB), at least for CCS measurements and oxides greater than about 5 nm. Improved TDDB is often achieved when carrier injection is from the substrate rather than from the electrode. The effect of grown-in crystalline defects on hard breakdown decreases with the decrease in dielectric film thickness. The temperature at which the wafers are annealed after poly deposition (for activation of the dopant in the poly) is important, e.g., TDDB of an MOS capacitor annealed at 1000°C is much better than that of the MOS capacitor annealed at 900°C. A wet, rather than a dry, oxidation has been noted to improve Q_{bd} (see Figure1). Finally, the effect of COPs on gate dielectric integrity decreases with the decrease in the oxide

thickness. Indications suggest that the effect of metal impurities be also reduced with decreasing oxide thickness [2], although this topic is still an open question with data reported for both possible outcomes.

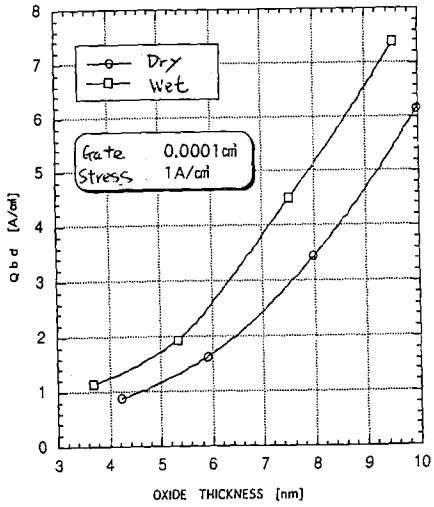

Fig.1. Qbd vs. oxide thickness for wet and dry oxidation. (The figure was supplied by Y.Murakami, Mitsubishi Materials Silicon Corporation).

As described elsewhere in this publication, the oxide wearout and breakdown field can be understood in terms of trap generation inside the oxide and locally high current regions occurring during the breakdown event. Both electric field and electron current contribute to the trap generation process through weakening of the oxide chemical bonds. Many effects occurring in oxides during high voltage stresses can be characterized by measuring the stress-generated trap densities, which are related to the stress-induced-leakage-current (SILC).

The literature [3-5] published on oxides and oxide breakdown mechanisms subsequent to this conference are included here for the interested reader.

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