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Ultra-Thin Film Dielectric Reliability Characterization

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Abstract: The reliability of gate oxides is becoming a critical concern as oxide thickness is scaled below 4 nm in future technology. The breakdown detection algorithms in traditional reliability characterization techniques must be modified for sub-4 nm thick SiO_2 films that exhibit excessive tunneling currents and soft breakdown. It becomes essential to fully understand the physical mechanism(s) responsible for gate oxide wear-out and breakdown if reliability projections are based on the results of highly accelerated wafer-level GOI tests. Issues relating to the reliability testing of ultra-thin oxides are discussed with examples.

Keywords: silicon oxide, reliability, accelerated stress tests, gate oxide integrity, dielectric breakdown

INTRODUCTION

Continued scaling of gate dielectric thickness for advanced CMOS technologies raises serious reliability concerns for ultra-thin oxides. Excessive leakage current and soft breakdown exhibited by ultra-thin dielectrics present new challenges for reliability characterization.

Device breakdown detection becomes very difficult as oxides become thinner due to soft or quasi-breakdown modes. The failure criteria used in traditional reliability tests must be modified to allow for dependable and robust detection of breakdown. This paper discusses the difficulty in obtaining reliability parameters for ultra-thin SiO_2 films.

Specifically, Section II discusses corrections necessary for estimating the oxide electric field in ultra-thin films. Section III presents examples of soft breakdown in several common breakdown tests and discusses new breakdown detection algorithms. The validity of a common metric in reliability characterization, charge-to-breakdown, is discussed in Section IV.

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Section V discusses reliability projections based on the results of highly accelerated breakdown tests. Finally, conclusions are given in Section VI.

DETERMINATION OF BREAKDOWN ELECTRIC FIELD

Determining the correct oxide electric field can be difficult for ultra-thin films due to excessive leakage current, gate electrode depletion and quantum effects.

A dominant feature of ultra-thin dielectrics is the presence of excessive leakage current at lower electric fields. This leakage is due to quantum mechanical "direct" tunneling and can become significant and be in excess of several A/cm^2 near device breakdown [1]. Figure 1 shows the tunneling current characteristics for a 3 nm, 5 nm, and 10 nm thick SiO_2 film. Note that the low-field direct-tunneling current is substantial for the 3 nm thick oxide.

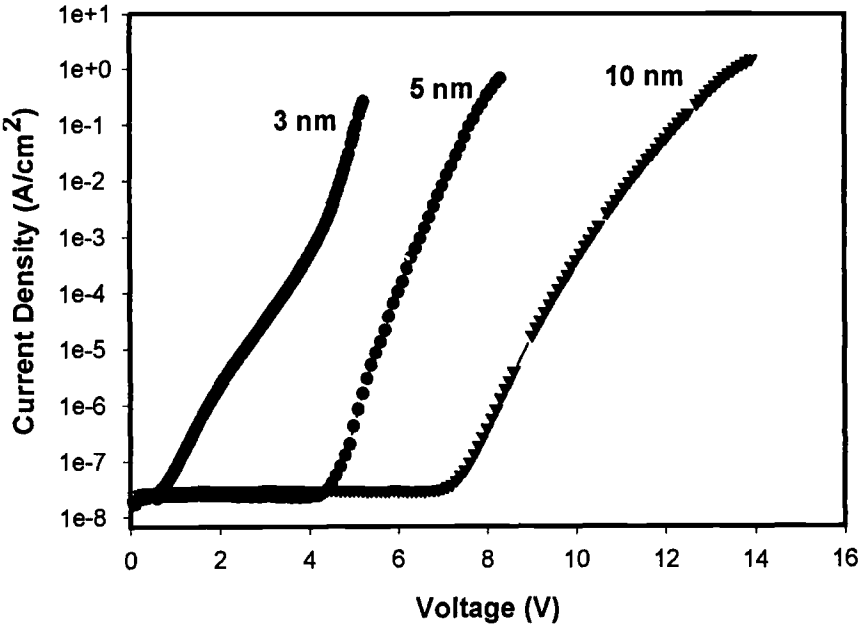

Figure 1- *Tunneling current versus voltage characteristics for a 3 nm, 5 nm, and 10 nm thick SiO_2 film. Note the substantial leakage current exhibited by the 3 nm film due to direct tunneling.*

Special care should be exercised when designing oxide test structures to reduce series resistance effects. The voltage drop across interconnects and gate electrodes due to excessive tunneling currents can be significant leading to an underestimation of gate electric field. Voltage drops can become large enough that the device breakdown voltage

is not achieved during the breakdown test. This is a particular concern for large-area test structures that can conduct significant levels of current before breakdown.

Other factors that can lead to incorrect estimates of oxide electric field include gate electrode depletion and quantum mechanical effects. The voltage applied across the gate can be divided into three components: the voltage drop across the gate-electrode depletion region, the gate oxide, and the quantum confinement region near the $Si\text{-}SiO_2$ interface. There is a variety of software codes and procedures available to estimate the oxide electric field when the above effects are significant and have been shown to yield similar results [2-4].

BREAKDOWN DETECTION IN GATE OXIDE INTEGRITY TESTS

Perhaps, the largest difficulty in conducting breakdown tests on ultra-thin oxides is the detection of the breakdown event. This event is usually described as a sudden decrease in voltage in the case of a constant-current test or a sudden increase in current in the case of a constant-voltage test. "Soft" or "quasi" breakdown modes are frequently observed when testing oxides thinner than 5 nm. This is illustrated in Fig. 2 which shows the voltage versus time characteristics for a 3, 10, and 20 nm oxide subjected to the Joint Electron Device Engineering Council (JEDEC) bounded current ramp test. Note that there are sudden and abrupt decreases in the gate voltage for the 10 nm and 20 nm thick films. However, the 3 nm thick film exhibits only a slight decrease in voltage. It is not clear where the actual breakdown occurred.

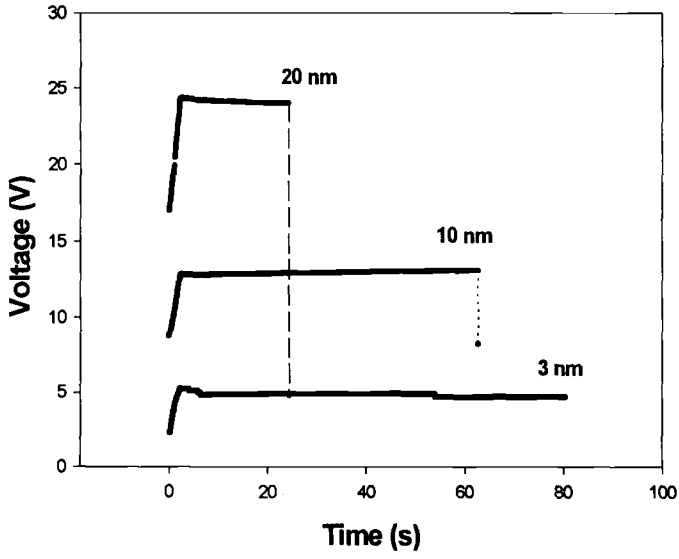

Figure 2- *Voltage versus time characteristics for a 3 nm, 10 nm, and 20 nm thick oxide subjected to a bounded-current ramp test. The current is ramped*

and held at 0 .25 A/cm^2. Breakdown is easily detected in the 10 nm and 20 nm thick films. The 3 nm thick film shows only a slight decrease in voltage making breakdown detection difficult. The device area is 5 x 10^{-4} cm^2.

Similar soft breakdown behavior is observed in constant-voltage tests illustrated in Fig. 3. The figure shows current versus time characteristics for a 3, 5, and 10 nm thick oxide subjected to a constant electric field of 13 MV/cm. The sudden increase in current is clearly observed for the 10 nm thick sample. However, breakdown is observed as a

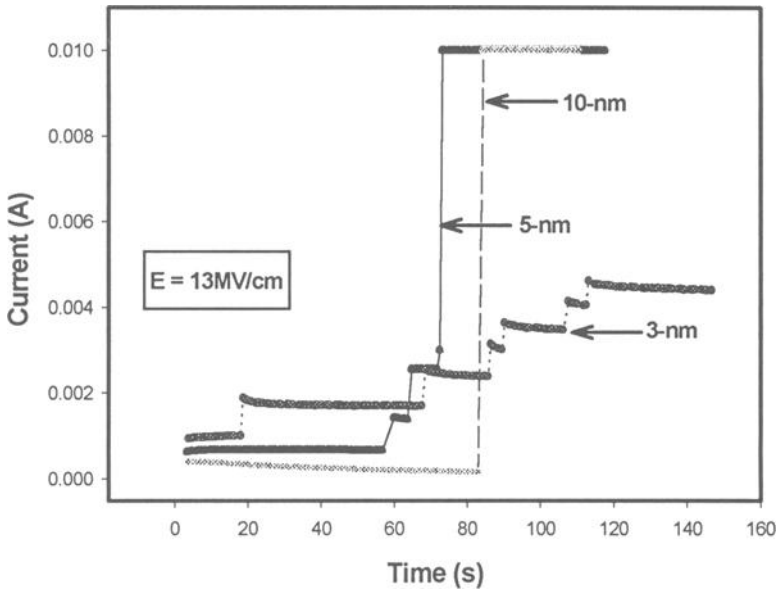

Figure 3- *Current versus time characteristics for a 3 nm, 5 nm, and 10 nm thick oxide subjected to a constant electric field of 13 MV/cm. Device breakdown exhibited by a sharp increase in current is clearly observed for the 10 nm thick sample. The 5 nm and 3 nm thick samples only show a series of small steps in current. The device area is 5 x 10^{-4} cm^2.*

series of small steps in current for the thinner films. JEDEC and American Society for Testing and Materials (ASTM) recently modified the voltage ramp test to utilize a change in slope as the breakdown criterion [5]. Earlier versions used an absolute current change or percent current change as the breakdown criterion. The ramp test is illustrated in Fig. 4 for three different oxide thicknesses. Breakdown is clearly observed for the 5 nm and 10 nm thick samples and can easily be detected by existing breakdown criteria. Note that breakdown is not evident in the 3 nm thick sample.

Figure 5 shows the slope ratio ($\Delta I(n)/\Delta V(n)$)/($\Delta I(n-1)/\Delta V(n-1)$) versus ramp voltage for the 3 nm sample. Note that a 3X increase in slope would be adequate to detect breakdown in this case.

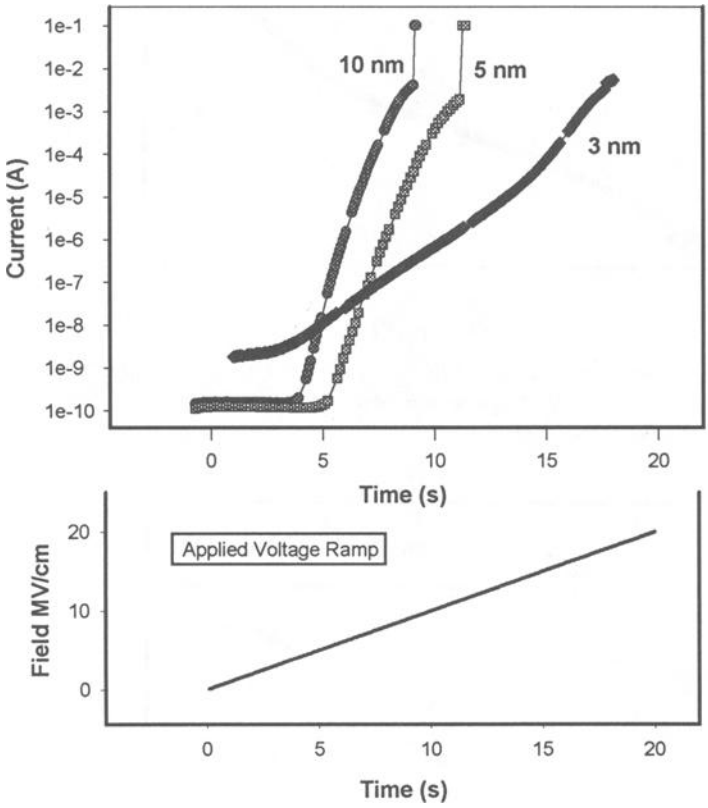

Figure 4- *Current versus voltage characteristics for a 3 nm, 5 nm, and 10 nm thick oxide subjected to the JEDEC/ASTM ramped voltage breakdown test. Breakdown in the 3 nm sample cannot be observed and requires a new criterion for detection.*

The process of evaluating the reliability of ultra-thin oxides on large area test structures is a particular concern. The structures can conduct significant current levels approaching the capabilities of the test system before failure. Breakdown detection can be difficult in this case since the difference between the current at breakdown and the tunneling current can be very difficult to detect. This is illustrated in Fig.6 which shows a figure identical to Fig.5, but the device has a larger area of 1×10^{-2} cm^2. In this case a 3X change in slope is not adequate to detect breakdown. Even if the change in slope ratio is reduced it is not clear where breakdown occurred.

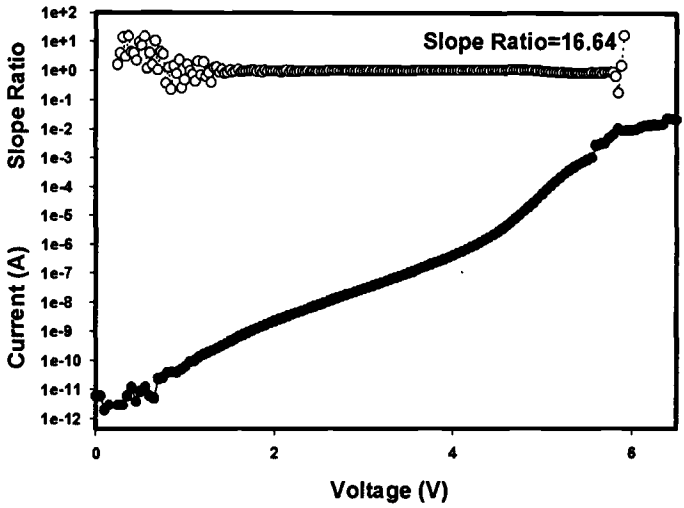

Figure 5- *Slope change ratio versus ramp voltage for a 3 nm thick oxide. Note that a 3X change in the slope would be adequate to detect breakdown. The device area is 5 x 10^{-4} cm^2.*

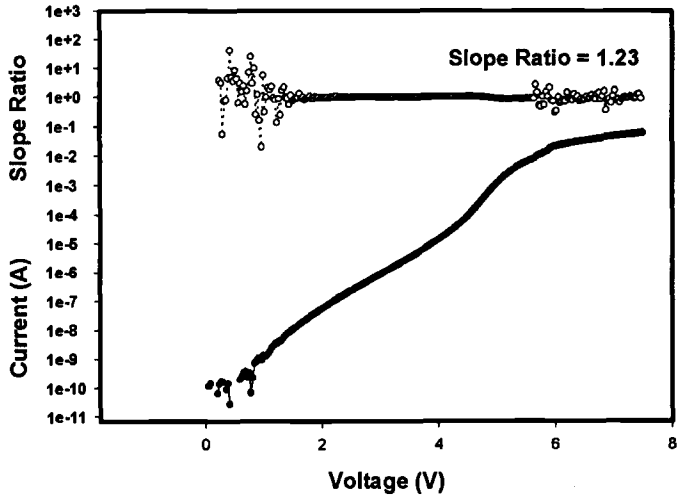

Figure 6- *Slope change ratio versus ramp voltage for a 3 nm thick oxide similar to Fig.5. In this case the device area is 1 x 10^{-2} cm^2. Note that a 3X change in the slope never occurs during the test.*

Figure 7 illustrates the effect a larger device area has on detecting failure during a bounded-current ramp test. The test is the JEDEC standard current-ramp test with a holding current of 0.25 A/cm. The bottom figure shows the voltage versus time characteristic for a 3 nm oxide with a 5 x 10^{-4} cm^2 area. Note that breakdown can be detected by the JEDEC failure criterion of 10% to 15% decrease in voltage.

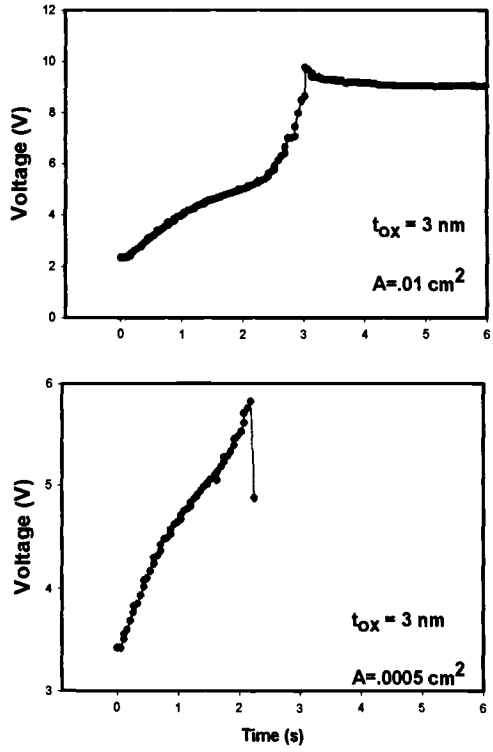

Figure 7- *Voltage versus time characteristic for the JEDEC J-RAMP test performed on a 3 nm oxide having an area of 1 x 10^{-2} cm^2 (Top) and an area of 5 x 10^{-4} cm^2 (Bottom). Breakdown is detected when the voltage across the oxide drops by 15%. Note that there is no voltage drop for the larger area device shown in the top figure.*

The top figure depicts the same oxide with an area of 1 x 10^{-2} cm^2. Note that there does not appear to be an abrupt drop voltage during the test. "Soft" or "quasi" breakdown has been explained as charge trapping and de-trapping in a physically damaged region near the Si-SiO_2 interface [6] or multiple tunneling paths caused by electron traps [7]. Another explanation is that the energy stored on the gate of an ultra-thin oxide (CV^2) is not large enough to cause a thermal destructive breakdown [8].

Recent studies have shown that soft breakdown is usually accompanied by current or voltage noise [9,10]. In fact, oxides thinner than 2.6 nm only exhibit noise when breakdown occurs [10]. Post-breakdown noise can increase by 5 orders of magnitude while pre and post current-voltage characteristics are nearly identical [11]. The monitoring of voltage or current noise to detect breakdown has been suggested as a new breakdown criterion in reliability tests [11,12]. This technique has been shown to be easily implemented in an automated testing environment [12]. Such a technique could possibly be used to detect breakdown in the examples shown in Figs. 6 and 7b.

It has been shown that soft breakdown in ultra-thin gate oxides does not immediately cause device failure (an increase in a metal-oxide-semiconductor field-effect transistor, MOSFET, offstate current) and is dependent on channel length and width [13].

THE VALIDITY OF CHARGE-TO-BREAKDOWN

Charge-to-breakdown (Q_{bd}) is one of the most common metrics used to monitor the integrity and reliability of thin-gate oxides. Q_{bd} can be obtained from any constant or ramped voltage/current breakdown test by integrating the current flowing through the dielectric until it fails. This procedure is illustrated in Fig. 8.

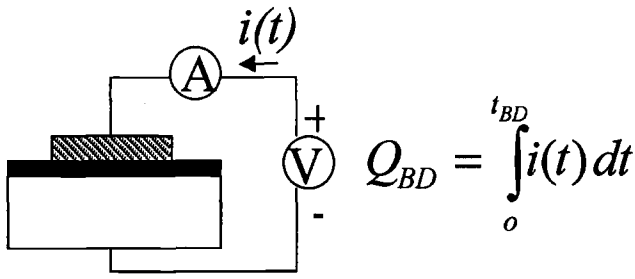

Figure 8- *Schematic of oxide breakdown test illustrating the calculation of charge-to-breakdown.*

Larger values of Q_{bd} are assumed to indicate more reliable and higher integrity dielectrics. Special care must be used when interpreting this value for ultra-thin dielectrics. It has been reported that Q_{bd} exhibits a dependence on stress current density [14,15]. This dependence on current density is observed to become greater as the oxide thickness is decreased [16]. Figure 9 shows that the value of Q_{bd} becomes smaller for thinner oxides when the stress current density is large (the right side region of the plot). However, this trend is the opposite for smaller stress current densities (the left side region of the plot). The value of Q_{bd} is independent of oxide thickness for moderate current densities (the center of the plot).

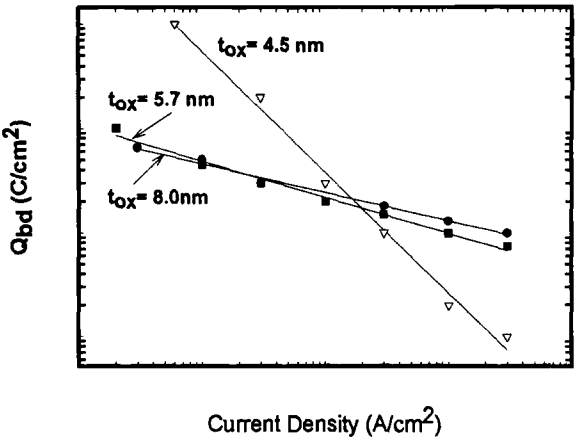

Figure 9- *Data from ref. 16 illustrating the increasing dependence of Q_{bd} on stress current density as oxide thickness is decreased.*

It has been observed that the value of Q_{bd} exhibits a dependence on test structure area. Q_{bd} decreases as the gate area increases. This dependence results from the localization of the breakdown spot and the statistical distribution of the location of this spot over the oxide gate area. Larger gate areas have a greater probability of including a breakdown spot. It has been recently reported that this dependence becomes greater as the gate oxide thickness is reduced [17]. This behavior is shown in Fig 10. Note that the value of Q_{bd} can vary up to three orders of magnitude depending on the test structure area for the 4.3 nm thick sample.

The variation of Q_{bd} with area is much less for the thicker films. The slope of the lines plotted in Fig. 10 is directly related to the dispersion of the failure distribution (or the shape parameter beta in a Weibull plot). Thinner oxides are reported to exhibit a larger beta in their Weibull distributions resulting in a larger variation with area [17, 18].

RELIABILITY EVALUATION

The primary motivation for performing accelerated breakdown tests is to monitor gate oxide integrity and quality and to ultimately obtain information that can be used to estimate product reliability in the field. Short-duration constant-current or voltage tests are usually used to obtain acceleration parameters to extrapolate oxide life under use conditions. Recent studies have questioned the use of constant current tests to evaluate ultra-thin oxides. Wu et al. [13] have shown that Q_{bd} or T_{bd} increases with decreasing oxide thickness under constant-current conditions and that the opposite trend occurs under constant-voltage conditions. It has been explained that a lower voltage is required to sustain the same current density in ultra-thin oxides due to the thickness dependence of direct tunneling currents.

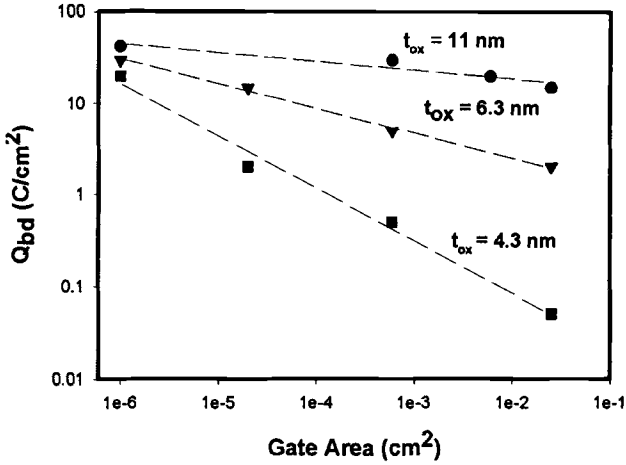

Figure 10- *Data reported in ref. 17 showing the area dependence of Q_{bd} for three different oxide thicknesses. Note that the thinnest oxide exhibits the largest variation of Q_{bd} with area.*

This lower voltage results in a lower electric field or a lower electron energy leading to a smaller defect generation rate. Nigam et al. [17] have also shown that constant current stressing can lead to an incorrect reliability assessment for ultra-thin dielectrics. Their example illustrates that using a constant-current stress (same current density) to evaluate the reliability between two different processes indicated each process had a similar charge-to-breakdown value. Constant-voltage tests revealed that there was a significant difference between the charge-to-breakdown values. It is generally believed that the results from accelerated constant-voltage tests are more accurate when assessing the reliability of thin films since devices operate in this mode during normal use conditions. Also, it has been shown that the $\log(Q_{bd})$ for ultra-thin dielectrics exhibits a linear dependence on gate voltage [19]. This observation suggests an "E" model [20] for breakdown, which predicts that the defect generation is electric field driven or related to the energy of the tunneling electrons, depending on the assumed physical mechanism.

It has been demonstrated that long-term time-dependent dielectric breakdown (TDDB) acceleration parameters can be extracted from any ramped voltage- or current-breakdown test by assuming that oxide damage is cumulative and irreversible during the test and the oxide electric field governs the defect generation [21]. Figure 11 illustrates the technique for a constant current breakdown test performed on a 9 nm oxide. The voltage-versus-time curve is recorded during the breakdown test. The curve can be divided into many smaller stress intervals and each interval removes a small percentage of the total life of the oxide as shown in the figure. The contributions from all of the intervals must add to unity when the device breaks down. Two parameters are required to construct the $\log(t_{50})$ vs. E curve used to extrapolate device life. These parameters are extracted from two distinct voltage-versus-time curves.

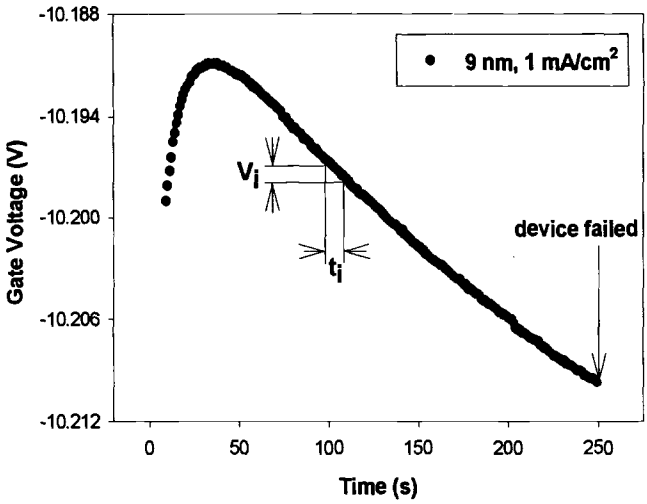

Figure 11- *Voltage-versus-time curve obtained during an accelerated constant current breakdown test for a 9 nm thick SiO_2 film. The figure illustrates the voltage-time integration technique for extracting long-term acceleration parameters from highly accelerated breakdown tests from ref. 21.*

The extracted $\log(t_{50})$ vs. E curve is shown with the actual curve determined from long-term time-dependent dielectric breakdown tests shown in Fig. 12. The agreement is excellent illustrating that the gate voltage or the oxide electric field governs the wear-out and eventual breakdown of thin dielectrics in the 3 nm to 9 nm thickness range.

CONCLUSIONS

The characterization of oxide reliability and integrity becomes more challenging as oxide thickness is scaled down. Soft breakdown modes dominate device failure and make breakdown detection very difficult. Failure detection algorithms in accelerated breakdown tests must be modified for ultra-thin dielectrics. Films thinner than 3 nm may require current or voltage noise detection techniques to detect breakdown.

Special care must be exercised when using charge-to-breakdown as a measure of device reliability. The value of Q_{bd} is a function of device area and current density. These dependencies become stronger as the oxide thickness is scaled down.

Constant-voltage tests are preferred when characterizing wear-out and time-dependent dielectric breakdown of ultra-thin dielectrics. This is due to the observation that defect generation is proportional to the gate voltage, and constant voltage is a more realistic stress condition.

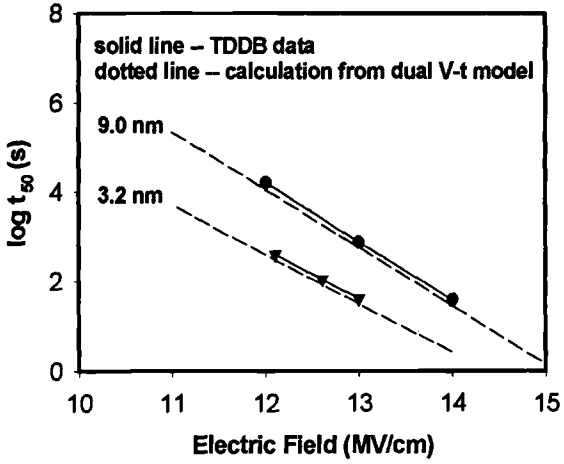

Figure 12- *Extracted log(t_{50}) vs. E curve using the technique in ref. 21 and compared to the actual curve obtained from time-dependent dielectric breakdown measurements.*

The log(t_{bd}) is observed to be linearly dependent on the oxide electric field, which is an important consideration when extrapolating device lifetime at use electric fields from accelerated stress conditions.

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