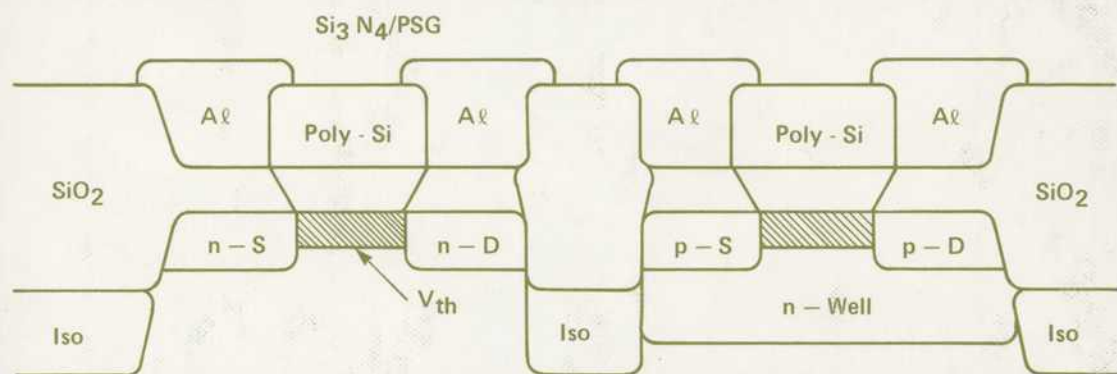


SILICON PROCESSING

D. C. GUPTA, editor



ASTM STP 804

SILICON PROCESSING

A symposium
sponsored by ASTM
Committee F-1 on Electronics,
National Bureau of Standards,
and Stanford University
San Jose, Calif., 19-22 Jan. 1982

ASTM SPECIAL TECHNICAL PUBLICATION 804
D. C. Gupta, Siliconix Incorporated, editor

ASTM Publication Code Number (PCN)
04-804000-46



1916 Race Street, Philadelphia, Pa. 19103

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Library of Congress Catalog Card Number: 82-83529

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Printed in Baltimore, Md. (b)
June 1983

Foreword

The Symposium on Silicon Processing was held in San Jose, California, on 19–22 January 1982. ASTM Committee F-1 on Electronics, the National Bureau of Standards, and Stanford University sponsored the symposium, and Dinesh C. Gupta, Siliconix Incorporated, presided as chairman. The Advisory Board consisted of Kenneth E. Benson, Bell Laboratories; W. Murray Bullis, Fairchild Advanced R&D Laboratory; Robert E. Lorenzini, Siltec Corporation; Samuel L. Marshall, Solid State Technology; and James D. Meindl, Stanford University. The Technical Committee consisted of Theodore I. Kamins, Hewlett-Packard Laboratories; Eric Mendel, International Business Machines; Krishna C. Saraswat, Stanford University; Joseph Stach, Penn State University; and Fritz G. Vieweg-Gutberlet, Wacker Chemitronic; and was headed by Paul H. Langer, Bell Laboratories. The Arrangements and Publicity Committee consisted of Austin R. Blew, Leighton Electronics Incorporated; Edward E. Gardner, IBM-GTD; Gilbert A. Gruber, Siliconix Incorporated; Charles Koehler, Fairchild Advanced R&D Laboratory; Donald J. Levinthal, Semiconductor International; Philip L. Lively, ASTM; David G. Mead, Nicolet Instrument Corporation; J. Timothy Raab, Rockwell International Recticon; Donald G. Schimmel, Bell Laboratories; and William R. Wheeler, Tencor Instruments; and was headed by Carl A. Germano, Motorola Incorporated. The Spouse Committee, consisting of Lou Ann Gruber, Vijay Gupta, and Carol Koehler, was headed by Kathleen Bullis; and the Registration Committee, consisting of Elaine Cohen, National Bureau of Standards, and Jan Meighan, San Jose Convention Bureau, was headed by Mr. Lively. We appreciate their efforts.

Appreciation is also extended to the following session and workshop chairmen: James T. Clemens, Bell Laboratories; James R. Ehrstein, National Bureau of Standards; Carl A. Germano, Motorola Incorporated; Gilbert A. Gruber, Siliconix Incorporated; Theodore I. Kamins, Hewlett-Packard Laboratories; William H. Kroeck, Western Electric Company; John W. Lampe, Martin Marietta Aerospace; Paul H. Langer, Bell Laboratories; Eric Mendel, International Business Machines; C. W. Pearce, Western Electric Company; R. Fabian W. Pease, Stanford University; Mike Powell, Motorola Limited; Sy Prussin, TRW Systems; Krishna C. Saraswat, Stanford University; Joseph Stach, Penn State University; and Fritz G. Vieweg-Gutberlet, Wacker Chemitronic.

Related ASTM Publications

Laser-Induced Damage in Optical Materials: 1979, STP 726 (1980),
04-726000-46

Lifetime Factors in Silicon, STP 712 (1980), 04-712000-46

Laser-Induced Damage in Optical Materials: 1978, STP 689 (1979),
04-689000-46

Optical Interferograms—Reduction and Interpretation, STP 666 (1979),
04-666000-46

Annual Book of ASTM Standards, Volume 10.04: Electronics (I),
01-100483-46

Annual Book of ASTM Standards, Volume 10.05: Electronics (II),
01-100583-46

A Note of Appreciation to Reviewers

The quality of the papers that appear in this publication reflects not only the obvious efforts of the authors but also the unheralded, though essential, work of the reviewers. On behalf of ASTM we acknowledge with appreciation their dedication to high professional standards and their sacrifice of time and effort.

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Preface

The papers in this volume were presented at the Symposium on Silicon Processing held in San Jose, California, on 19–22 January 1982. The symposium was sponsored by ASTM Committee F-1 on Electronics, the National Bureau of Standards, and Stanford University. In addition to the technical presentations, the symposium included well-attended workshops on each technical topic; impressions of these workshops are provided in Appendix II.

The trend towards very-large-scale integration (VLSI) is usually described as increasing device count on an integrated circuit chip. The associated trends towards smaller feature size, larger chip size, and larger wafer diameter present new problems in processing technology and control to the semiconductor device manufacturer. The symposium was designed to identify the future directions in materials and processing technology required for VLSI and areas where additional measurement development and standardization are required to accelerate the efficient implementation and control of these technologies.

The symposium opened with a series of brief talks on the role of standards and on the work performed by the Stanford Center for Integrated Systems, the National Bureau of Standards, and the National Science Foundation in relation to the semiconductor industry. These talks were followed by an overview projection of future VLSI technology which emphasized the need for rigorous and disciplined control of processes to achieve the potential of VLSI. These talks are presented in Appendix I.

The opening general session included a discussion on semiconductor business and education requirements in the Eighties by a panel of prominent individuals in industry, academia, and government. Brief summaries of the panel responses to key questions are provided in Appendix II.

The response to the symposium was extremely favorable, suggesting a continuing need for a regular forum to discuss technology topics in the context of measurement and control. Accordingly, the symposium sponsors have initiated plans both to repeat the symposium at two-year intervals and to broaden industry involvement in the organization and conduct of future symposia. The present symposium has established a consistent theme for these symposia as they evolve: understanding and control of the complex process technologies required for VLSI and other advanced device concepts. The problem areas and standardization needs identified in this and subse-

quent symposia will provide the feedback to the research community and voluntary standards system essential for the future growth of the industry.

We appreciate the cooperation and support of the ASTM staff in the formulation of these proceedings. The assistance of W. Murray Bullis is acknowledged. Finally, we are indebted to our industrial, government and university colleagues who contributed to the content of the symposium and the proceedings.

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